What is claimed is:

1. A method of manufacturing a field effect transistor having a semiconductor substrate with a main surface, comprising:

forming a conductive layer on the main surface via a dielectric film;

forming a gate electrode by etching the conductive layer using a mask formed thereon;

forming a source region and a drain region in the main surface; and

forming pocket regions in the semiconductor substrate by implanting ion using the mask.

2. A method of manufacturing a field effect transistor as recited in claim 1, wherein the mask has a desired width to defined gate length and the implanting process is carried out so as to head from an obliquely upward direction of the mask to the semiconductor substrate using the mask.

3. A method of manufacturing a field effect transistor as recited in claim 1, wherein the mask has a width being less than a desired width to defined gate length and the implanting process is carried out so as to head from an upward direction of the mask to the semiconductor substrate using the mask.

4. A method of manufacturing a filed effect transistor as recited in claim 3, wherein a dielectric spacer is formed on a side wall of the mask after the implanting process and then the gate electrode is formed by etching the conductive layer using the mask with the dielectric spacer.

5. A method of manufacturing a field effect transistor as recited in claim

3, wherein the gate electrode is formed so as to expand a width from a top surface to a bottom surface after the implanting process.

6. A method of manufacturing a field effect transistor as recited in claim 1, wherein the pocket regions is formed so as to underlie the gate electrode pocket regions.

7. A method of manufacturing a field effect transistor having a semiconductor substrate with a main surface, comprising:

forming a conductive layer on the main surface via a dielectric film;

forming a mask on the conductive layer;

forming pocket regions in the semiconductor substrate by implanting ion using the mask;

forming a gate electrode by etching the conductive layer using the mask;

forming a source region an a drain region in the main surface using the gate electrode as a mask; and

wherein the pocket regions underlying the source and drain regions.

8. A method of manufacturing a field effect transistor as recited in claim 7, wherein the mask has a desired width to defined gate length and the implanting process is carried out so as to head from an obliquely upward direction of the mask to the semiconductor substrate using the mask.

9. A method of manufacturing a field effect transistor as recited in claim 7, wherein the mask has a width being less than a desired width to defined gate length and the implanting process is carried out so as to head from an

upward direction of the mask to the semiconductor substrate using the mask.

10. A method of manufacturing a field effect transistor as recited in claim 9, wherein a dielectric spacer is formed on a sidewall of the mask after the implanting process and then the gate electrode is formed by etching the conductive layer using the mask with the dielectric spacer.

11. A method of manufacturing a field effect transistor as recited in claim 9, wherein the gate electrode is formed so as to expand a width from a top surface to a bottom surface after the implanting process.

12. A method of manufacturing a field effect transistor as recited in claim 7, wherein the pocket regions is formed so as to underlie the gate electrode, pocket regions.

13. A method of manufacturing a field effect transistor including a gate electrode formed on a semiconductor substrate, a pair of first impurity regions for a source and a drain formed on both sides of said gate electrode on said semiconductor substrate and a pair of second impurity regions formed between said pair of first impurity regions used to inhibit an expansion of a deletion layer expanding from one impurity region making up said pair of first impurity regions toward the other impurity region making up said pair of first impurity regions, formed at an interval and exhibiting a conductive property being different from that of said first impurity region, said method comprising:

a process of forming a conductive layer for a gate electrode on said semiconductor substrate;

a process of forming an etching mask for said gate electrode on said conductive layer and removing unwanted portions from said conductive layer using photolithography; and

a process of implanting an impurity used to form said second impurity region in a predetermined region in said semiconductor substrate existing under said conductive layer by an ion implantation method using said etching mask as a mask for said ion implantation.

14. The method of manufacturing the field effect transistor according to Claim 13, wherein said etching mask has a desired width to define a gate length and wherein an ion is implanted at an angle formed by a line heading from an obliquely upward direction of said etching mask to a downward portion of said etching mask and then to an inside of said semiconductor substrate and a line being vertical to a surface of said semiconductor substrate.

15. The method of manufacturing the field effect transistor according to Claim 13, wherein said etching mask has a width being less than a desired width defining a gate length and wherein said ion is implanted at a right angle formed by a line heading from an upward direction of said etching mask to said inside of said semiconductor substrate and a line being vertical to said surface of said semiconductor substrate.

16. The method of manufacturing the field effect transistor according to Claim 15, wherein side walls are formed on said etching mask, after said ion implantation, to substantially provide said desired width to said gate electrode and, by using said etching mask containing said side walls as a

resist mask, unwanted portion is removed from said conductive layer and said gate electrode defining a predetermined gate length is formed.

17. The method for manufacturing the field effect transistor according to Claim 15, wherein, after said ion implantation using said etching mask, by performing etching processing using said etching mask as a resist mask, said gate electrode whose width is increased along the downward direction to secure said predetermined gate length.